**California State University, Northridge**

**College of Engineering & Computer Science**

**Electrical and Computer Engineering Department**

**ECE 443L Digital Electronics Laboratory Report 10**

**CMOS based Phase Lock Loop Circuit Design, Simulation and Experimental Test as well as Analysis**

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**Abstract:**

A phase lock loop (PLL) is a controlled system which generates output signals with relative phase to the input. There are several different types of phase lock loop systems, but the most common includes frequency oscillators and a phase detector. Students create a phase lock loop system on PSpice to generate similar inputs and outputs.

**Key Terms:**

Phase Lock Loop, Oscillator, Frequency, Phase

**Simulation and Experimental Result:**

Diagram, schematic

Description automatically generated

Figure 10.1: CASE 1 CLAYTON Phase Lock Loop Schematic, Vin = 1kHz

Table

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Figure 10.2: CASE 1 CLAYTON Phase Lock Loop Simulation Result, Vin = 1kHz

Diagram, schematic

Description automatically generated

Figure 10.3 CASE 1 EVAN Phase Lock Loop Schematic, Vin = 2kHz

Graphical user interface, chart, application, table, Excel

Description automatically generated

Figure 10.4: CASE 1 EVAN Phase Lock Loop Simulation, Vin = 2kHz

Diagram, schematic

Description automatically generated

Figure 10.5: CASE 2 HAROUTUN Phase Lock Loop Schematic, Vin = 10kHz

Chart

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Figure 10.6: CASE 2 HAROUTUN Phase Lock Loop Simulation Result, Vin = 10kHz

Diagram, schematic

Description automatically generated

Figure 10.7: CASE 3 CLAYTON Phase Lock Loop Schematic, Vin = 10kHz

Chart

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Figure 10.8: CASE 3 CLAYTON Phase Lock Loop Simulation Result, Vin = 10kHz

Diagram, schematic

Description automatically generated

Figure 10.9: CASE 3 EVAN Phase Lock Loop Schematic, Vin = 15kHz

Graphical user interface, chart, application, table, Excel, line chart

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Figure 10.10: CASE 3 EVAN Phase Lock Loop Simulation Result, Vin = 15kHz

Diagram, schematic

Description automatically generated

Figure 10.11: CASE 4 HAROUTUN Phase Lock Loop Schematic, Vin = 20kHz

Graphical user interface, chart, application, table, Excel, line chart

Description automatically generated

Figure 10.12: CASE 4 HAROUTUN Phase Lock Loop Simulation Result, Vin = 20kHz

**Conclusion:**

In this experiment, students are exposed to the functionality of a phase lock loop system. PLL systems are common systems in electronics as it is simple and outputs an output phase waveform in respect to the input phase waveform.